IN THE CLAIMS

Please cancel claim 49 without prejudice.

Please amend the following claims which are pending in the present application:

1-45. (Cancelled)

46. (Previously presented) A method of making an interposer, comprising:

forming an oxide layer on each of a first surface and a second surface of a substrate;

patterning the oxide layer of the first surface to expose a first portion and a second portion of the substrate;

isotropically etching through the first portion of the exposed substrate to form a first portion of at least one deep-via opening;

anisotropically etching through the second portion of the exposed substrate to form a second portion of the at least one deep-via opening;

growing an oxide layer on inner surfaces of the at least one deep-via opening;

sputtering a copper barrier layer and a copper seed layer into the first and second portions of the at least one deep-via opening after growing the oxide layer;

electroplating a conductive material over the seed layer to form the at least one deep-via; and

forming vias and interconnect lines over the second surface of the substrate.

47. (Currently amended) The method of claim 46 wherein the interconnect lines are electrically coupled to the at least one deep-via opening.

48. (Currently amended) The method of claim 46 wherein the oxide layer is thermally grown to a thickness of approximately 0.5[[μ]]um.

49. (Cancelled)

50. (Previously presented) The method of claim 46 wherein the copper barrier layer is of a thickness in a range of 10-50 nm.

51. (Currently amended) The method of claim 46 wherein the copper seed layer [[layer]] is of a thickness in a range of 100-300 nm.

52. (Previously presented) The method of claim 46 further comprising depositing a copper layer over the first surface of the substrate.

53. (Previously presented) The method of claim 46 further comprising:

forming a silicon nitride layer over the second surface of the substrate;

depositing an oxide layer superjacent to the silicon nitride layer;

patterning the oxide layer to expose portions of the silicon nitride layer;

etching the exposed portions of the silicon nitride layer;

depositing a copper barrier layer and a copper seed layer over the second surface of the substrate; and

electroplating a conductive material over the copper seed layer.

54-55. (Withdrawn)